

**Appl. No. 09/881,299**

### **REMARKS**

Claims 47-51 and 53-59 are pending in the application with claims 47-51, 53, 55-57, and 59 amended herein and claim 52 canceled herein.

Claims 47-51, 53, 54, and 55-59 stand rejected under 35 USC 102(e) as being anticipated by Tobben. Applicants request reconsideration.

Amended claim 47 sets forth an integrated circuit including, among other features, a layer comprising copper over a semiconductive substrate and a layer of intermetallic material within the layer comprising copper. The intermetallic material layer includes copper and palladium and has a thickness of from about 50 to about 150 Angstroms. A conductive connection is on the intermetallic layer. Tobben does not disclose or suggest an intermetallic layer containing copper and palladium. Tobben does not disclose or suggest an intermetallic layer having a thickness of from about 50 to about 150 Angstroms.

Since Tobben does not disclose every element of claim 47, Tobben does not anticipate claim 47. Claims 48-51, 53, and 54 depend from claim 47 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed.

Amended claim 55 sets forth an integrated circuit that includes, among other features, a layer comprising Cu over a semiconductive substrate, a layer of alloy material within the layer comprising Cu, and a conductive connection on the alloy layer. The alloy layer includes intermetallic  $\text{Cu}_3\text{Pd}$  and has a thickness of from about 50 to about 150 Angstroms. As can be appreciated from the claim 47 discussion above, Tobben does not disclose or suggest intermetallic  $\text{Cu}_3\text{Pd}$ . Tobben further does not disclose or suggest an

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intermetallic thickness of from about 50 to about 150 Angstroms. At least for such reason, claim 55 is not anticipated. Claims 56-58 depend from claim 55 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed.

Amended claim 59 sets forth an integrated circuit that includes, among other features, a layer consisting of copper over a semiconductive substrate, a layer of intermetallic material over the copper layer, and a conductive connection on the intermetallic layer. The intermetallic layer consists of copper and palladium and has a thickness of from about 50 to about 150 Angstroms. As indicated above, Tobben does not disclose or suggest an intermetallic layer consisting of copper and palladium. Tobben also does not disclose or suggest an intermetallic layer thickness of from about 50 to about 150 Angstroms. At least for such reasons, Tobben does not anticipate claim 59.

Claims 55-58 stand rejected under 35 USC 102(e) as being anticipated by Havemann. Applicants request reconsideration.

The subject matter of amended claim 55 is described above. Page 4 of the Office Action admits that Havemann does not disclose intermetallic material including copper and palladium. Accordingly, claim 55 and its dependents, claims 56-58, are not anticipated.

Claim 52 stands rejected under 35 USC 103(a) as being unpatentable over Tobben in view of Obeng. Claim 52 is canceled herein.

Claims 47-54 and 59 stand rejected under 35 USC 103(a) as being unpatentable over Havemann in view of Obeng. Applicants request reconsideration.

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The subject matter of amended claim 47 is discussed above. Pages 3 and 4 of the Office Action allege that Havemann discloses an alloy material thickness of between about 100 to 200 Angstroms. However, col. 3, lns. 48-55 of Havemann reveal that disclosure is only provided of a blanket deposition of 100-200 Angstroms of silicon nitride, not an intermetallic. The clear wording applies the thickness only to silicon nitride and does not expressly describe a thickness for  $\text{Cu}_3\text{Ti}$ .

Also, Havemann expressly describes converting the  $\text{Cu}_3\text{Ti}$  to  $\text{TiN}$ . Since the intermetallic of Havemann is converted to  $\text{TiN}$ , Havemann cannot be considered to disclose or suggest the claimed thickness of intermetallic material. Any intermetallic is merely an intermediate and if some suggestion of a thickness for other than silicon nitride may be implied, then such thickness would be for  $\text{TiN}$ , not an intermetallic. Further, because  $\text{Cu}_3\text{Ti}$  is converted, Havemann does not disclose a conductive connection to an intermetallic layer, as claimed.

Obeng is relied upon as allegedly disclosing  $\text{Cu}_3\text{Pd}$ , but fails to remedy the deficiencies of Havemann discussed above. Since both references are deficient in the same respects, combination cannot be considered to somehow disclose or suggest a feature missing from both. Claim 47 is thus patentable. Claims 48-51, 53 and 54 depend from claim 47 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

The subject matter of amended claim 59 is discussed above. Amended claim 59 sets forth a conductive connection on an intermetallic layer consisting of copper and

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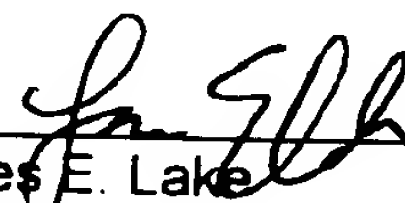
palladium and having a thickness of from about 50 to about 150 Angstroms. Accordingly, claim 59 is also patentable.

Applicants herein set forth adequate reasons for allowance of claims 47-51 and 53-59 over the cited references. Applicants request allowance of all pending claims in the next Office Action.

Respectfully submitted,

Dated: 17 Oct 2002

By: \_\_\_\_\_

  
James E. Lake  
Reg. No. 44,854

**Appl. No. 09/881,299**

Application Serial No. .... 09/881,299  
Filing Date ..... June 13, 2001  
Inventor ..... Dinesh Chopra, et al  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2814  
Examiner ..... P. Cao  
Attorney's Docket No. .... MI22-1747  
Title: Conductive Connection Forming Methods, Oxidation Reducing Methods, and  
Integrated Circuits Formed Thereby

**VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
PRELIMINARY AMENDMENT ACCOMPANYING A RCE FILING**

**In the Claims**

The claims have been amended as follows. Underlines indicate insertions and  
~~strikeouts~~ indicate deletions.

47. (twice amended) An integrated circuit comprising:
- a semiconductive substrate;
  - a layer comprising ~~a first metal~~ copper over the substrate;
  - a layer of ~~alloy~~ intermetallic material within the layer comprising ~~the first metal~~  
copper, the ~~alloy~~ intermetallic material layer comprising ~~the first metal and a second~~  
~~metal different from the first metal, the second metal comprising~~ copper and palladium,  
~~magnesium, or both~~ and having a thickness of from about 50 to about 150 Angstroms;
  - and
  - a conductive connection on the ~~alloy~~ intermetallic layer.

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48. (twice amended) The integrated circuit of claim 47 wherein the alloy

intermetallic material consists of an intermetallic.

49. (amended) The integrated circuit of claim 47 wherein the alloy intermetallic

material is less susceptible to formation of metal oxide compared to ~~the first metal~~

copper.

50. (amended) The integrated circuit of claim 47 wherein the ~~first metal comprises~~

layer comprising copper consists of copper aside from the intermetallic material layer.

51. (amended) The integrated circuit of claim 47 wherein the alloy intermetallic

material consists ~~essentially of the first and second metals~~ of copper and palladium.

53. (amended) The integrated circuit of claim 47 wherein about ~~50 to about 300~~ 150

Angstroms of the ~~first metal~~ layer comprising copper is alloy intermetallic material.

55. (amended) An integrated circuit comprising:

a semiconductive substrate;

a layer comprising Cu over the substrate;

a layer of alloy material within the layer comprising Cu, the alloy material layer  
comprising intermetallic ~~Cu<sub>3</sub>Ti~~ Cu<sub>3</sub>Pd and having a thickness of from about 50 to about

150 Angstroms; and

a conductive connection on the alloy layer.

56. (amended) The integrated circuit of claim 55 wherein the alloy material consists

~~essentially of Cu<sub>3</sub>Ti~~ Cu<sub>3</sub>Pd.

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57. (amended) The integrated circuit of claim 55 wherein about 50 to about 300 150 Angstroms of the first metal layer comprising Cu is alloy material.

59. (amended) An integrated circuit comprising:

a semiconductive substrate;

a layer consisting of copper over the substrate;

a layer of alloy intermetallic material ~~within~~ over the copper layer, the alloy intermetallic material layer consisting of copper and a second metal, the second metal consisting of palladium, magnesium, or both and having a thickness of from about 50 to about 150 Angstroms; and

a conductive connection on the alloy intermetallic layer.

**-END OF DOCUMENT-**